WHAT IS CLAIMED IS:

1. A pipeline operator comprising:

at least a first processing stage and a second processing stage;

latching units provided at input stage, between processing stages and at output stage of the first processing stage and the second processing stage respectively, which latching units hold processing data and processing results;

a first processing unit provided at the first processing stage, which first processing unit carries out a processing according to an instruction by using the processing data held in the latching unit on the upstream side and for outputting the processing result to the latching unit on the downstream side;

a second processing unit provided at the second processing stage, which second processing unit carries out a processing according to an instruction by using the processing data held in the latching unit on the upstream side and for outputting a processing result to the latching unit on the downstream side; and

instruction decoding units for decoding the instructions dispatched to the first processing unit and the second processing unit respectively, wherein

in decoding the instruction dispatched to the second processing unit, each instruction decoding unit decodes the

instruction as the instruction to pass the processing data held in the latching unit on the upstream side through the first processing unit.

2. A pipeline operator comprising:

at least a first processing stage and a second processing stage;

latching units provided at input stage, between processing stages and at output stage of the first processing stage and the second processing stage respectively, which latching units hold processing data and processing results;

a first processing unit provided at the first processing stage, which first processing unit carries out a processing according to an instruction by using the processing data held in the latching unit on the upstream side and for outputting the processing result to the latching unit on the downstream side;

a second processing unit provided at the second processing stage, which second processing unit carries out a processing according to an instruction by using the processing data held in the latching unit on the upstream side and for outputting a processing result to the latching unit on the downstream side; and

instruction decoding units for decoding the instructions dispatched to the first processing unit and the second

processing unit respectively, wherein

in decoding the instruction dispatched to the first processing unit, each instruction decoding unit decodes the instruction as the instruction to pass the processing result of the first processing unit held in the latching unit on the upstream side through the second processing unit.

3. A pipeline operator comprising:

first to n-th (n is a natural number such that n > 1) processing stages;

latching units provided at input stage, between processing stages and at output stage of the first to n-th processing stages, which latching units hold processing data and processing results;

first to n-th processing units provided at the first to n-th processing stages respectively, which processing unit carries out a processing according to an instruction by using the processing data held in the latching unit on the upstream side and for outputting the processing result to the latching unit on the downstream side; and

instruction decoding units for decoding the instructions dispatched to the first to n-th processing units respectively, wherein

in decoding the instruction dispatched to an x-th (x is a natural number such that x > 1) processing unit, each

instruction decoding unit decodes the instruction as the instruction to pass the processing data held in the latching unit on the upstream side through the first processing unit to the (x-1)-th processing unit.

4. A pipeline operator comprising:

first to n-th (n is a natural number such that n > 1) processing stages;

latching units provided at input stage, between processing stages and at output stage of the first to n-th processing stages, which latching units hold processing data and processing results;

first to n-th processing units provided at the first to n-th processing stages respectively, which processing unit carries out a processing according to an instruction by using the processing data held in the latching unit on the upstream side and for outputting the processing result to the latching unit on the downstream side; and

instruction decoding units for decoding the instructions dispatched to the first to n-th processing units respectively, wherein

in decoding the instruction dispatched to an x-th (x is a natural number such that n > x) processing unit, each instruction decoding unit decodes the instruction as the instruction to pass the processing result of the x-th processing

unit held in the latching unit on the upstream side through the (x+1)-th processing unit to the n-th processing unit.

5. A pipeline operator comprising:

at least a first processing stage and a second processing stage;

latching units provided at input stage, between processing stages and at output stage of the first processing stage and the second processing stage respectively, which latching units hold processing data and processing results;

a first processing unit provided at the first processing stage, which first processing unit carries out a processing according to an instruction by using the processing data held in the latching unit on the upstream side and for outputting the processing result to the latching unit on the downstream side;

a second processing unit provided at the second processing stage, which second processing unit carries out a processing according to an instruction by using the processing data held in the latching unit on the upstream side and for outputting a processing result to the latching unit on the downstream side; and

instruction decoding units for decoding the instructions dispatched to the first processing unit and the second processing unit respectively, wherein

the instruction decoding units decode the instructions that have a correlation between the processing of the first processing unit and the processing of the second processing unit that the processing result of the first processing unit becomes the processing data of the second processing unit, and further, in decoding the instruction to the second processing unit for executing the processing by itself, the instruction decoding unit decodes the instruction as the instruction to pass the processing data held in the latching unit on the upstream side through the first processing unit.

6. A pipeline operator comprising:

at least a first processing stage and a second processing stage;

latching units provided at input stage, between processing stages and at output stage of the first processing stage and the second processing stage respectively, which latching units hold processing data and processing results;

a first processing unit provided at the first processing stage, which first processing unit carries out a processing according to an instruction by using the processing data held in the latching unit on the upstream side and for outputting the processing result to the latching unit on the downstream side;

a second processing unit provided at the second

processing stage, which second processing unit carries out a processing according to an instruction by using the processing data held in the latching unit on the upstream side and for outputting a processing result to the latching unit on the downstream side; and

instruction decoding units for decoding the instructions dispatched to the first processing unit and the second processing unit respectively, wherein

the instruction decoding units decode the instructions that have a correlation between the processing of the first processing unit and the processing of the second processing unit that the processing result of the first processing unit becomes the processing data of the second processing unit, and further, in decoding the instruction to the first processing unit for executing the processing by itself, the instruction decoding unit decodes the instruction as the instruction to pass the processing result of the first processing unit held in the latching unit on the upstream side through the second processing unit.

7. A pipeline operator comprising:

first to n-th (n is a natural number such that n > 1) processing stages;

latching units provided at input stage, between processing stages and at output stage of the first to n-th

processing stages, which latching units hold processing data and processing results;

first to n-th processing units provided at the first to n-th processing stages respectively, which processing unit carries out a processing according to an instruction by using the processing data held in the latching unit on the upstream side and for outputting the processing result to the latching unit on the downstream side; and

instruction decoding units for decoding the instructions dispatched to the first to n-th processing units respectively, wherein

the instruction decoding units decode the instructions that have a correlation between m (m is a natural number such that n > m) stages of processing from an r-th (r is a natural number such that r > 1) processing unit to an s-th (s is a natural number such that r < s ≤ n) processing unit out of the first processing unit to the n-th processing unit that the processing result of the pre-stage processing unit becomes the processing data of the next-stage processing unit, and further, in decoding the instruction to an x-th (x is a natural number such that r ≤ x ≤ s) processing unit among the r-th processing unit to the s-th processing unit for executing the processing by the x-th processing unit by itself, the instruction decoding units decode the instructions as the instructions to pass the processing results held in the latching unit on the upstream

side through the first processing unit to the (x-1)-th processing unit.

8. A pipeline operator comprising:

first to n-th (n is a natural number such that n > 1) processing stages;

latching units provided at input stage, between processing stages and at output stage of the first to n-th processing stages, which latching units hold processing data and processing results;

first to n-th processing units provided at the first to n-th processing stages respectively, which processing unit carries out a processing according to an instruction by using the processing data held in the latching unit on the upstream side and for outputting the processing result to the latching unit on the downstream side; and

instruction decoding units for decoding the instructions dispatched to the first to n-th processing units respectively, wherein

the instruction decoding units decode the instructions that have a correlation between m (m is a natural number such that n > m) stages of processing from an r-th (r is a natural number such that r > 1) processing unit to an s-th (s is a natural number such that r < s < n) processing unit out of the first processing unit to the n-th processing unit that the processing

result of the pre-stage processing unit becomes the processing data of the next-stage processing unit, and further, in decoding the instructions to an x-th (x is a natural number such that $r \leq x \leq s$) processing unit to an (x+p)-th (p is a natural number such that $p \leq s-r$) processing unit among the r-th processing unit to the s-th processing unit for completing the execution of one processing by the processing units of p stages, the instruction decoding units decode the instructions as the instructions to pass the processing data held in the latching unit on the upstream side through the first processing unit to the (x-1)-th processing unit.

9. A pipeline operator comprising:

first to n-th (n is a natural number such that $n > 1$) processing stages;

latching units provided at input stage, between processing stages and at output stage of the first to n-th processing stages, which latching units hold processing data and processing results;

first to n-th processing units provided at the first to n-th processing stages respectively, which processing unit carries out a processing according to an instruction by using the processing data held in the latching unit on the upstream side and for outputting the processing result to the latching unit on the downstream side; and

instruction decoding units for decoding the instructions dispatched to the first to n-th processing units respectively, wherein

the instruction decoding units decode the instructions that have a correlation between m (m is a natural number such that n > m) stages of processing from an r-th (r is a natural number such that r > 1) processing unit to an s-th (s is a natural number such that r < s < n) processing unit out of the first processing unit to the n-th processing unit that the processing result of the pre-stage processing unit becomes the processing data of the next-stage processing unit, and further, in decoding the instruction to an x-th processing unit (x is a natural number such that $r \leq x \leq s$) among the r-th processing unit to the s-th processing unit for the x-th processing unit to execute the processing by itself, the instruction decoding units decode the instructions as the instructions to pass the processing result of the x-th processing unit held in the latching unit on the upstream side through the (x+1)-th processing unit to the n-th processing unit.

10. A pipeline operator comprising:

first to n-th (n is a natural number such that n > 1) processing stages;

latching units provided at input stage, between processing stages and at output stage of the first to n-th

processing stages, which latching units hold processing data and processing results;

first to n-th processing units provided at the first to n-th processing stages respectively, which processing unit carries out a processing according to an instruction by using the processing data held in the latching unit on the upstream side and for outputting the processing result to the latching unit on the downstream side; and

instruction decoding units for decoding the instructions dispatched to the first to n-th processing units respectively, wherein

the instruction decoding units decode the instructions that have a correlation between m (m is a natural number such that $n > m$) stages of processing from an r-th (r is a natural number such that $r > 1$) processing unit to an s-th (s is a natural number such that $r < s < n$) processing unit out of the first processing unit to the n-th processing unit that the processing result of the pre-stage processing unit becomes the processing data of the next-stage processing unit, and further, in decoding the instructions to an (x-p)-th processing unit to an x-th (x and p are natural numbers such that $r \leq x \leq s$ and $p \leq s-r$) processing unit among the r-th processing unit to the s-th processing unit for completing the execution of one processing by the processing units of p stages, the instruction decoding units decode the instructions as the instructions to pass the

processing results of the (x-p)-th processing unit to the x-th processing unit held in the latching unit on the upstream side through the (x+1)-th processing unit to the n-th processing unit.

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